In the Claims:

1. (Currently Amended) An integrated circuit arrangement ~~(10)~~ comprising:~~,~~

~~having~~ at least one metallization layer ~~(16)~~ containing a multiplicity of electrically conductive interconnects ~~(14),~~;

~~having~~ an interconnect dielectric ~~(18)~~ between the interconnects ~~(14),~~;

~~having~~ electrically conductive interconnect intermediate material ~~(20)~~ arranged in each case between a side area ~~(40)~~ of an interconnect ~~(14)~~ and the interconnect dielectric ~~(18),~~;

~~having~~ a multiplicity of electrically conductive connecting sections ~~(12)~~ which in each case form a section of an electrically conductive connection to or from an interconnect ~~(14),~~;

~~having~~ a connecting section dielectric ~~(24)~~ between the connecting sections ~~(12)~~; and~~,~~

~~having~~ connecting section intermediate material ~~(28)~~ arranged in each case at least one of between a connecting section ~~(12)~~ and the connecting section dielectric ~~(24)~~ and/~~or~~ between a connecting section ~~(12)~~ and an interconnect ~~(14)~~,

wherein the interconnect intermediate material ~~(20)~~ and the connecting section intermediate material ~~(28)~~ ~~making~~ makes contact with one another at at least one connection ~~(12)~~.

2. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in claim 1, wherein~~,~~ at least one of:

at the connection, the interconnect intermediate material ~~(20)~~ and the connecting section intermediate material ~~(28)~~ make contact at two or three or four side areas ~~(40)~~ of an interconnect~~;~~ ~~(14)~~ and/~~or~~

~~wherein~~ the interconnect intermediate material ~~(20)~~ and the connecting section intermediate material ~~(28)~~ make contact at an edge ~~(42)~~ formed by ~~the~~ a contact line of two side areas of the interconnect ~~(14)~~.

3. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in claim 1 ~~or 2~~, wherein at least one of:

the interconnect ~~(14)~~ has a constriction ~~(72, 82, 112, 132)~~ at the connecting section ~~(12)~~, the width ~~(B3, B4, B7, B8)~~ of said constriction being chosen such that contact regions are produced at opposite side areas of the interconnect ~~(14)~~, and/~~or wherein~~

the constriction ~~(72, 112)~~, along the longitudinal axis of the interconnect ~~(14)~~, has a length ~~(L1, L2)~~ that is less than five times or less than three times the width ~~(B3, B7)~~ of the constriction ~~(72, 112)~~.

4. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in claim 3, wherein at least one of: the connecting section ~~(12)~~ is arranged at ~~the~~ an end of the interconnect ~~(14)~~, and/~~or wherein~~ the constriction ~~(112, 132)~~ has the form of a wedge or the form of a step.

5. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in claim 3, wherein at least one of: the interconnect ~~(14)~~ extends in at least two different directions from the connecting section ~~(12)~~, and/~~or~~ each end of ~~wherein~~ the constriction ~~(72, 82), at its ends, in each case~~ has the form of a wedge or the form of a step.

6. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in claim 1 ~~or 2~~, wherein at least two sections of the same interconnect ~~(14)~~ or of different interconnects are wider than the connecting sections ~~(12)~~ at the connecting sections ~~(12)~~, and wherein the contact regions are situated at ~~such~~ side areas of the sections whose normal directions are situated transversely or oppositely with respect to one another.

7. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in ~~one of the preceding claims~~claim 1, wherein at least one of:

the interconnect ~~(14)~~ comprises copper, ~~or~~ a copper alloy containing at least ninety-five percent copper, ~~and/or wherein the interconnect (14) comprises~~ aluminum, or ~~or~~ an aluminum alloy containing at least ninety-five percent aluminum,

~~and/or wherein~~ at least one of the interconnect dielectric ~~(18)~~ and/~~or~~ the connecting section dielectric contains an oxide~~, preferably silicon dioxide,~~ or a dielectric having a dielectric constant of less than 3.9,

~~and/or wherein~~ at least one of the interconnect intermediate material ~~(20)~~ and/~~or~~ the connecting section intermediate material ~~(28)~~ contains a nitride, ~~preferably comprises a nitride, in particular made of a metal nitride,~~

~~and/or wherein~~ the interconnect intermediate material contains a refractory metal ~~or comprises a refractory metal~~, ~~preferably made of tantalum,~~ and

~~and/or wherein~~ the connecting sections ~~(12)~~ contain tungsten~~,~~ ~~preferably comprise tungsten, or wherein the connecting sections (12) contain copper or comprise~~ or copper.

8. (Currently Amended) The circuit arrangement ~~(10)~~ as claimed in ~~one of the preceding claims~~claim 1, wherein ~~the~~ at least one of:

an area of an interconnect ~~(14)~~ that is adjacent to a connecting section ~~(12)~~ is ~~essentially free and/or more~~ than eighty percent free of an electrically conductive intermediate material, and/~~or~~ ~~wherein~~

the circuit arrangement ~~(10)~~ has been fabricated by means of a damascene technique or by means of a dual damascene technique.

9. (Currently Amended) A method for generating design data for the production of an integrated circuit arrangement ~~(10), in particular of a circuit arrangement (10) as claimed in one of the preceding claims~~, ~~having the steps that are~~the method being performed without restriction by the order specified and with the aid of an apparatus ~~(200)~~:

~~predefinition (304) of~~ predefining design data that determine the geometrical arrangement of interconnects ~~(14)~~ in a metallization layer ~~(16)~~ and of connecting sections ~~(12)~~ which in each case form a section of an electrically conductive connection to or from an interconnect ~~(14),~~;

~~predefinition (304) of~~ predefining at least one rule for altering the design data, the application of the rule to the design data giving rise to changed design data that determine a changed arrangement of the

interconnects ~~(14)~~ and the connecting sections ~~(12)~~, and the number of contact locations of interconnect intermediate material ~~(20)~~ between an interconnect ~~(14)~~ and an interconnect dielectric ~~(18)~~ and of connecting section intermediate material ~~(28)~~ between a connecting section ~~(28)~~ and a connecting section dielectric ~~(18)~~ being increased in a targeted manner in comparison with the original arrangement by application of the rule~~,~~;

automatically applying ~~application (310) of~~ the rule to the design data, generating the changed design data ~~being generated~~, and at least one of outputting ~~(316) and/or storage of~~ and storing the changed design data.

10. (Currently Amended) The method as claimed in claim 9, ~~wherein~~ further comprising at least one of:

reducing~~in accordance with one rule,~~ the width of a pattern for an interconnect ~~(14), in particular in an overlap region with a pattern for a connecting section (12), is reduced~~in accordance with one rule, ~~preferably in wedge-shaped or stepped fashion, and/or wherein,~~ and

displacing ~~in accordance with another rule,~~ at least one of a pattern for an interconnect ~~(14)~~ and~~/or~~ a pattern for a connecting section ~~(12) is displaced~~ in a design plane in accordance with another rule.

11. (Currently Amended) A program ~~(354)~~ having an instruction sequence whose execution by a data processing system ~~(320)~~ has the effect of performing a method as claimed in claim 9 ~~or 10~~.

12. (Currently Amended) An apparatus ~~(320), in particular a data processing system,~~ for generating design data, the apparatus comprising: ~~in particular according to a method as claimed in claim 9 or 10,~~

~~having~~ an access unit for accessing design data that determine the geometrical arrangement of interconnects ~~(14)~~ in a metallization layer ~~(16)~~ and of connecting sections ~~(12)~~ which in each case form a section of an electrically conductive connection to or from an interconnect ~~(14)~~;~~,~~

~~having~~ a unit ~~(324)~~ which stores at least one rule for altering the design data, the application of the rule to the design data giving rise to changed design data that determine a changed arrangement of interconnects ~~(14)~~ and connecting sections ~~(12)~~, and the number of contact locations of

interconnect intermediate material ~~(20)~~ between an interconnect ~~(14)~~ and an interconnect dielectric ~~(18)~~ and of connecting section intermediate material ~~(28)~~ between a connecting section ~~(28)~~ and a connecting section dielectric ~~(18)~~ being increased in a targeted manner in comparison with the original arrangement by application of the rule; and~~,~~

~~and having~~ a processing unit ~~(326, 328)~~, which automatically applies the rule to the design data, the changed design data being generated.

13. (New) The circuit arrangement as claimed in claim 7, the oxide comprises contains silicon dioxide.

14. (New) The circuit arrangement as claimed in claim 7, wherein the nitride comprises a metal nitride.

15. (New) The circuit arrangement as claimed in claim 7, wherein the refractory metal comprises tantalum.

16. (New) The method as claimed in claim 10, wherein the pattern comprises an overlap region of the interconnect with a pattern for a connecting section.

17. (New) The method as claimed in claim 10, wherein the pattern is reduced in wedge-shaped or stepped fashion.